Amendments to of Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor apparatus, comprising:

a support substrate made of a semiconductor substrate having through holes filled with conductor in conformity with a first uniform pitch,

a capacitor formed on or above said support substrate,

a wiring layer formed on or above said support substrate, leading some of said through holes filled with conductor upwards via said capacitor, having branches, and having wires of a second uniform pitch narrower than said first uniform pitch, and

plural semiconductor elements disposed on or above said wiring layer, having terminals in conformity with the second uniform pitch, and connected with said wiring layer via said terminals.

Claim 2 (Previous Presented): The semiconductor apparatus, according to claim 1, further comprising a circuit board having wiring of a first uniform pitch and connected to lower surfaces of said through holes filled with conductor.

Claim 3 (Canceled).

Claim 4 (Previously Presented): The semiconductor apparatus, according to claim 1, wherein said support substrate is a Si substrate having through holes with an insulation film formed on the side walls of the holes, and said through holes filled with conductor are metallic conductors packed in said through holes.

Claim 5 (Previously Presented): The semiconductor apparatus, according to claim 2, wherein said support substrate is a Si substrate having through holes with an insulation film formed on the side walls of the holes, and said through holes filled with conductor are metallic conductors packed in said through holes.

Claim 6 (Original): The semiconductor apparatus, according to claim 4, wherein said insulation film is a silicon oxide film formed by thermal oxidation, and upper and lower surfaces of said silicon substrate are also covered with a silicon oxide film.

Claim 7 (Original): The semiconductor apparatus, according to claim 1, wherein said capacitor is a decoupling capacitor connected between power wires, and said wiring layer has branches between said decoupling capacitor and at least one of said semiconductor elements.

Claim 8 (Previously Presented): The semiconductor apparatus, according to claim 1, wherein said through holes filled with conductor include a first signal wire; said wiring layer contains a second signal wire for leading the first signal wire substantially vertically; and said capacitor has electrodes with a vacancy around a region where said second signal wire is located.

Claim 9 (Previously Presented): The semiconductor apparatus, according to claim 5, wherein said through holes filled with conductor include a first signal wire; said wiring layer contains a second signal wire for leading the first signal wire substantially vertically; and said capacitor has electrodes with a vacancy around a region where said second signal wire is located.

Claim 10 (Original): The semiconductor apparatus, according to claim 1, further comprising an insulation layer disposed on said support substrate, having a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, and insulating said wiring layer and said capacitor.

Claim 11 (Original): The semiconductor apparatus, according to claim 1, wherein said capacitor has a capacitor dielectric layer made of an oxide containing at least one of Ba, Sr and Ti, and a pair of capacitor electrodes sandwiching the capacitor dielectric layer and containing at least partially one of Pt, Ir, Ru, Pd or any of their oxides.

Claim 12 (Original): The semiconductor apparatus, according to claim 9, wherein said capacitor has a capacitor dielectric layer made of an oxide containing at least one of Ba, Sr and Ti, and a pair of capacitor electrodes sandwiching the capacitor dielectric layer and containing at least partially one of Pt, Ir, Ru, Pd or any of their oxides.

Claim 13 (Original): The semiconductor apparatus, according to claim 1, wherein said wiring layer contains a wiring connecting said plural semiconductor elements with each other.

Claim 14 (Original): The semiconductor apparatus, according to claim 1, further comprising another circuit part connected with said wiring layer.

Claim 15 (Withdrawn): A process for producing a semiconductor apparatus, comprising the steps of:

(a)forming through holes at a first pitch in a support substrate;

(b)forming an insulation layer on side walls of said through holes;

(c) filling through holes with conductor in the through holes provided with said insulation film;

(d) forming a capacitor connected with at least some of said through holes filled with conductor, and wires connected with said through conductor or said capacitor and having a second pitch, on said support substrate, and

(e)connecting plural semiconductor elements having terminals in conformity with said second pitch, with said wires.

Claim 16 (Withdrawn): The process for producing a semiconductor apparatus, according to claim 15, wherein said support substrate is a Si substrate;

said step (a) thermally oxidizes both surfaces of the Si substrate to form silicon oxide films, and forms through holes passing from one of the silicon oxide films through the silicon substrate to reach the other silicon oxide film;

said step (b) thermally oxidizes side walls of the through holes; and

said step (c)forms a seed layer on back surface of the other silicon oxide film, and removes oxide films at bottoms of the through holes, to expose the seed layer, and forms a plating layer in the through holes using said seed layer as seed.

Claim 17 (Withdrawn): The process for producing a semiconductor apparatus, according to claim 16, wherein said step (d) forms a lower electrode layer, patterns the lower electrode layer to form signal wires and vacancies around them, forms an oxide dielectric film covering the lower electrode, patterns the oxide dielectric film to expose the signal wires and connecting portion of the lower electrode, forms an upper electrode layer covering the oxide dielectric film, and patterns the upper electrode layer to form signal wires, a wire connected with the lower electrode and vacancies around the wires.

Claim 18 (Withdrawn): The process for producing a semiconductor apparatus, according to claim 17, wherein said step (d) further alternately forms an insulation layer and a wiring layer to form a wiring layer adapted to a second pitch.

Claim 19 (Withdrawn): The process for producing a semiconductor apparatus, according to claim 18, wherein said step (d) forms a wiring layer containing wires connecting plural semiconductor elements with each other.

Claim 20 (Withdrawn): The process for producing a semiconductor apparatus, according to claim 15, further comprising the step of connecting said support substrate with a circuit board having wires adapted to said first pitch.